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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,469	01/06/2004	Jeong-won Lee	Q77017	2348

23373 7590 04/05/2005

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EXAMINER	
NGUYEN, LINH V	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,469	LEE ET AL.	
	Examiner	Art Unit	
	Linh V. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application No. 10/751,469 filed on 01/06/2004. Claims 1 – 6 are pending on this application.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 3, 5 and 6 are rejected under 35 U.S.C. 102(e) as being anticipate by Tsuchiya U.S. Patent No. 6,812,781.

Regarding claim 1, Fig. 2 of Tsuchiya discloses a amplifier circuit, comprising: an input circuit ([16, 18], [36, 38]) part for outputting a differential current (output current of

18, and output current of 38) proportional to differentiations of input voltages (Vin); a bias circuit part ([12, 14]; [32, 34]) for mirroring the differential current, inverting the differential current, and producing an inverted differential current (output current of 16 and output current 36); and an output circuit part ([C1, R1, 50], [C2, R2, 52]) for adjusting each magnitude of the differential current and the inverted differential current based on a predetermined ratio size of MOS transistors of the output circuit part (50, 52 are predetermines size MOS transistor), to output an adjusted differential current (output current of 50) and an adjusted inverted differential current (output current of 52), adding the adjusted differential current and the adjusted inverted differential current (at the Node of Vout), and producing an output current in a push-pull form (50 and 52 disclose the current at output node in push-pull form [Vdd-Vss]).

Regarding claim 2, wherein the input circuit part includes: a first differentiation circuit (16, 18) for being inputted with a reference voltage (voltage at input gate of 18) and a first input voltage (Vin at input gate of 16) of the input voltages, and outputting a first differential current (current at the drain of 18); a second differentiation circuit (36, 38) for being inputted with the reference voltage (voltage at input gate of 38) and a second input voltage (Vin at input gate of 36) of the input voltages, and outputting a second differential current (output current of 38); and a current mirror circuit (34, 32) for mirroring the first and second differential currents.

Regarding claim 3, wherein the first and second differentiation circuits each has respective fully differential operational amplifier, capacitors, and resistors (Fig. 2).

Regarding claim 5, wherein the bias circuit part (12, 14, 32, 34)

Mirrors (12, 14) the first differential current (output current of 18) and produces a first inverted differential current (output current of 18) wherein the first differential current is inverted, and mirrors (32, 34) the second differential current (output current of 38) and produces a second inverted differential current (output current of 36) wherein the second differential current is inverted.

Regarding claim 6, wherein the output circuit part includes (C1, C2, R1, R2, 50, 52): a first output part (C1, R1, 50) for adjusting each magnitude of the first differential current and the second inverted differential current based on the predetermined size ratio of a first MOS transistor (50) and adding (Node at 16) the adjusted magnitudes of the first differential current and the second inverted differential current (Current input to gate 50), thereby outputting a first output current (output current of 50); and a second output part (R2, C2, 52) for adjusting each magnitude of the second differential current and the first inverted differential current based on the predetermined size ratio of a second MOS transistor (52) and adding (Node at 36) the adjusted magnitudes of the second differential current and the first inverting differential current (Current input to Gate 52) , thereby outputting a second output current (output current of 52), and the output current (Iout at node Vout) being produced by adding (Node at Vout) the first and second output currents (output currents of 5-0 and 52).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuchiya as applied to claim 3 above.

Tsuchiya as applied to claim 3 above, discloses the fully differential operational amplifier has input terminals formed with MOS transistors in a left (16) to right (18) symmetry, except for the input MOS transistors are bipolar transistors. It would have been obvious to one having ordinary sill in the art at the time the invention was made to implement the differential input transistors of Tsuchiya by bipolar transistor, since it was know in the art that differential input bipolar transistors or MOS input transistor is a common know knowledge in the art for implementing differential amplifier.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (571) 272-1810. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (571) 272-1812. The fax phone numbers for the organization where this application or proceeding is assigned are

(703-872-9306) for regular communications and (703-872-9306) for After Final communications.

3/28/05

Linh Van Nguyen

Art Unit 2819